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Design and Analysis of 60ghz Frequency Divider using MCML Logic

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***Abstract*—High speed and low power are the main challenges in modern VLSI design. The proposed paper presents swift frequency divider circuit using MCML (MOS Current Mode Logic). The divider operates up to 60GHZ clock frequency. The implementation is carried by using 45nm cadence virtuoso tool. The presented logic consumes 2.5mW from 1.2V supply. The phase noise of the proposed frequency divider is 150dBc/Hz at 60GHz offset.**

***Index Terms*— Frequency divider, Low power, MCML, 60GHz.**

I. INTRODUCTION

Swift frequency divider circuits are required for many applications ranging from frequency synthesizer in wireless communication to quadrature signal generation and clock revival in high speed serial links, RF instrumentation and OFC. The high speed low power and elevated sensitivity divider is the key ingredient for these listed applications. To achieve this specification MCML architecture is sizably used owing to its high speed. The MCML has important characteristics as high static power consumption owing to its consistent operating current. In this paper design and analysis of synchronous frequency divider circuit using T flip flop (master slave) is presented. To build synchronous frequency divider the main ingredients such as MS T-flip flop and AND gate is used. To achieve elevated speed these components are built by using MCML logic. The design is implemented using 45nm cadence virtuoso tool.

Compared to conventional DFF divider the proposed divider operates at high frequency. The proposed divider operates up to highest frequency of 60GHZ. Till date, the maximum operating frequencies is reported with bipolar technologies[1], [2], the maximum drawback is their high power consumptions. Compared to the BJT dividers, metal oxide semiconductor (CMOS) dividers are always operate at less frequency. To increase the operating frequency using MOS for a desired power consumption, plenty of methods are used, such as injection-locking [3], dynamic circuit [4], and improved Miller dividers [5].

Compared to dynamic MOS divider, static divider has a increased operating range and average operating frequency for desired power consumption. Static frequency dividers operating around 20 GHz using CMOS has recently presented [6]–[9], but the architecture is mainly suffering from increased power. In this paper, by idealizing the transistors size, a low power high frequency dividers using MCML logic is presented. The tradeoff between the speed and power consumption is debated in detail.

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A. MCML

MOS Current Mode Logic has few advantages.

1. Due to differential nature, they have high noise immunity.
2. Achieves high speed consuming less power
3. High supply noise rejection

MCML employs differential topology to reduce environmental and power supply noise. Basic MCML block diagram is depicted in figure 1. It has two load devices with PMOS as diode connected load, two input NMOS transistors and current mirror which acts as current source. PMOS load is forced to work in ohmic region of operation. Channel resistance of PMOS along with the biased current through it determines the voltage swing at the output. The required logic deduction is implemented with two input NMOS transistors. The current mirror is accustomed to provide a constant current through the circuit so as to reduce variations from the power lines and maintains uniform power consumption irrespective of change in clock frequency. For high speed operation, NMOS transistors of MCML circuit are forced to operate in saturation region.

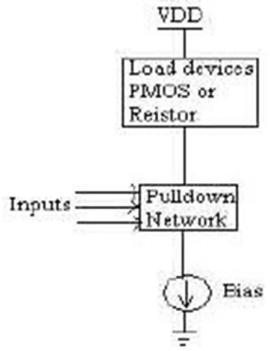

Figure 1 Basic MCML block

B. Circuit Design

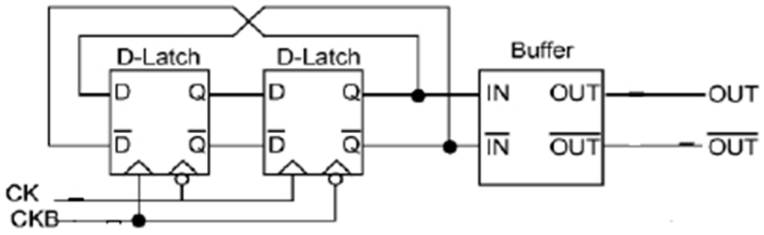

Figure 2 frequency divider

Figure 2 shows the logical diagram of 2:1 static frequency divider using MOS Current Mode Logic [11]. The divider is based on classic master slave T flip flop in which inverted slave outputs are connected to master inputs. The differential behavior of MCML provides reduced switching noise and increased noise margin. Separate buffers are used to provide maximum voltage swing. The Master section of Master slave flip-flop constructed by using MCML logic is outlined in Figure 3. The master consists of evaluate stage (M1 –M7) and latch stage of (M10-M12). The current source of conventional MCML logic is omitted [6] for reduced voltage operation. At high frequency, there is a big overlap when both evaluate and latch stage is turned on. This makes the supply current to be relatively constant and in turn this limits the switching noise.

Figure 4 depicts the slave section of Master Slave Flip-Flop using MOS Current Mode Logic. The evaluate stage of slave section consists of M15 to M17 and latch stage holds M18 to M20. To reduce the propagation delay of the divider circuit the W/L of PMOS (load transistors) is made as minimum as possible.

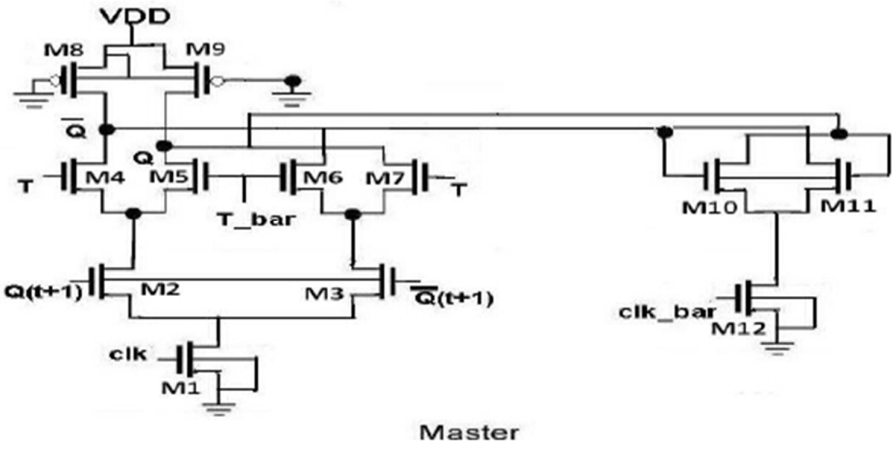

Figure 3 Master section of MS flip flop

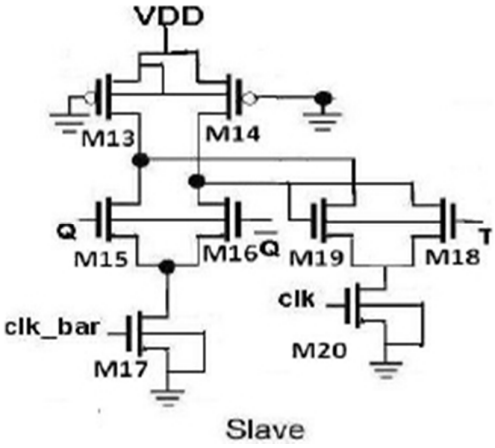

Figure 4 Slave section of MS FF

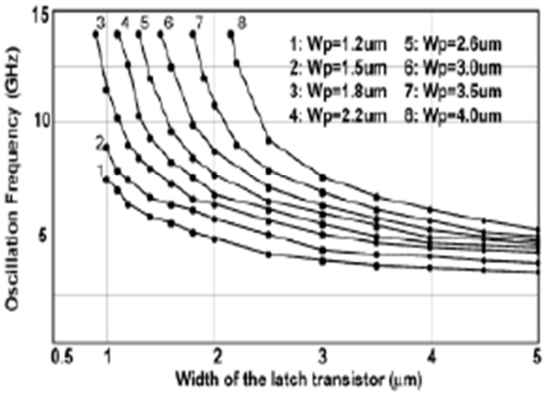

Figure 5 Plots of oscillation frequencies versus the width of the Latch transistors with different PMOS load

Figure 5 shows the graph of frequency as a function of varying sizing of PMOS loads. From the graph it is clear that smaller load transistor leads to lower oscillation frequency, because Rl increases with smaller load. One more important concept of the divider circuit is for a given load transistor, the frequency of operation is reduced with increased latch transistor width. It is also important to note that output voltage swing of the divider circuit increases with increase in the width of latch transistors because of larger negative capacitance of cross coupled transistor.

II. Experimental Results

To perform the measurements easier and more realistic, a 8:1 circuit consisting of three stages of 2:1 divider is implemented. The circuit is implemented in 45-nm cmos logic process. The test bench of the proposed 2:1 and 8:1frequency divider is depicted in figure 6a and 6b respectively.

The input frequency for 8:1 frequency divider is 60GHz and output frequency are 30GHz, 15GHz and 7.5GHz respectively. The input output waveforms of presented logic are depicted in figure 7. Figure 8 shows the waveform of DC analysis of output voltage of static frequency divider for different values of Vdd. Table I summarizes the few early reported 2:1 CMOS static frequency divider with respect to power consumption and operating frequency. The 2.5-mW power consumption is very minimum at 60 GHz if compared with other bulk CMOS dividers [7]–[9] and is close to that of the silicon-on-insulator (SOI) CMOS frequency divider [10].

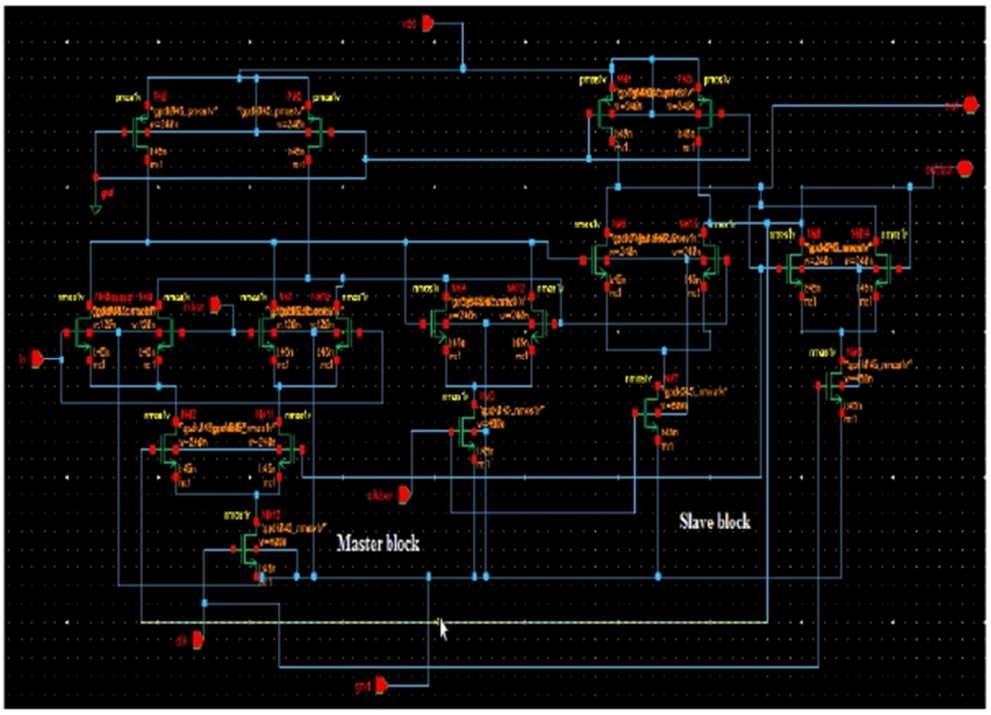

Figure 6a Block of 2:1 frequency divider

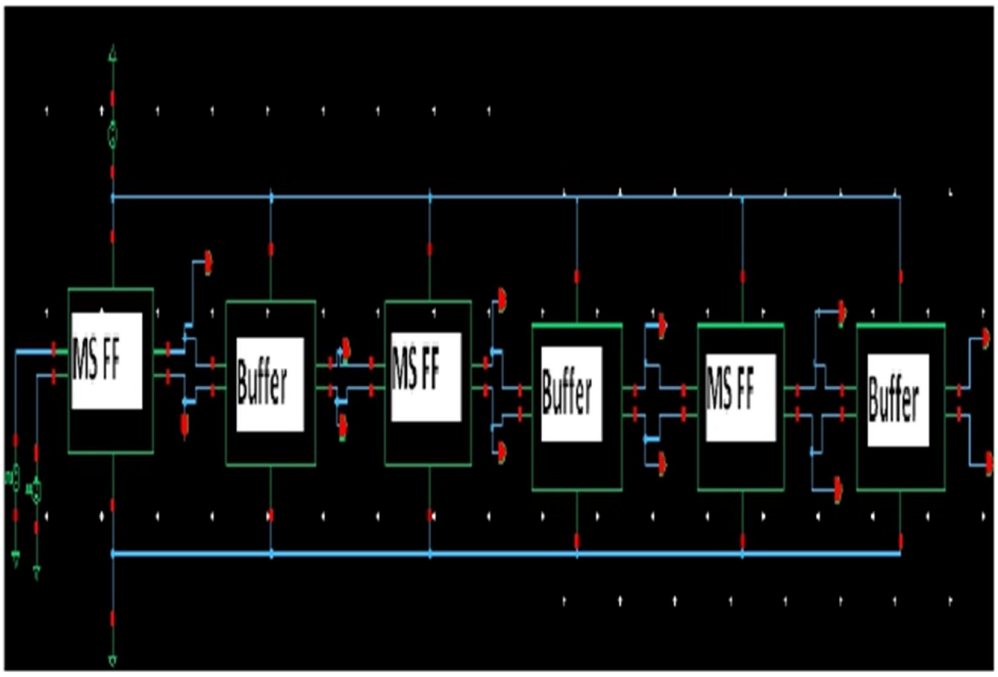

Figure 6b Block of 8:1 frequency divider

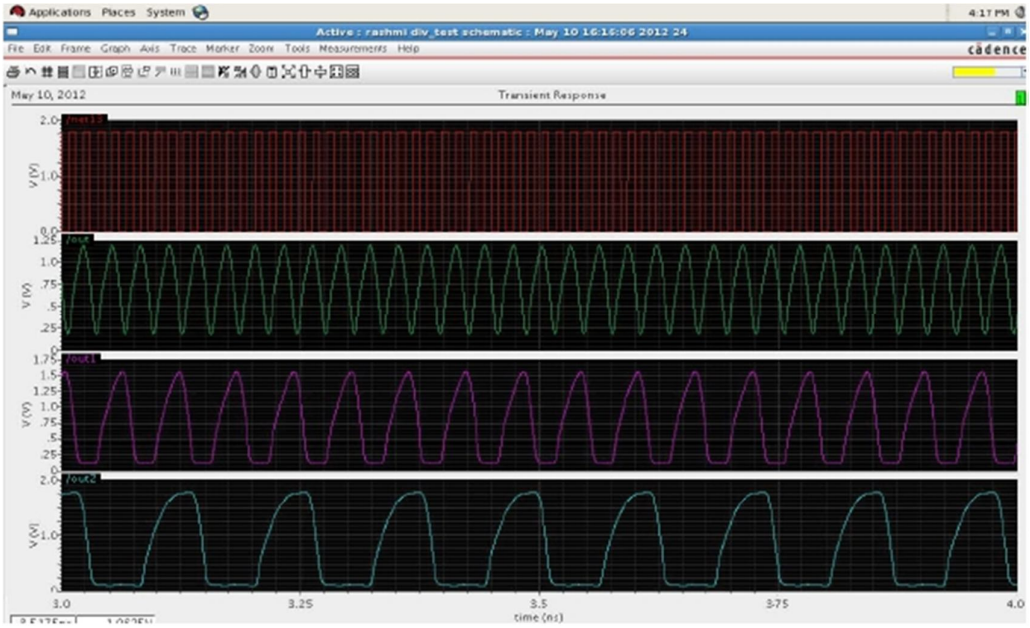

Figure 7 input output waveforms 8:1 static divider

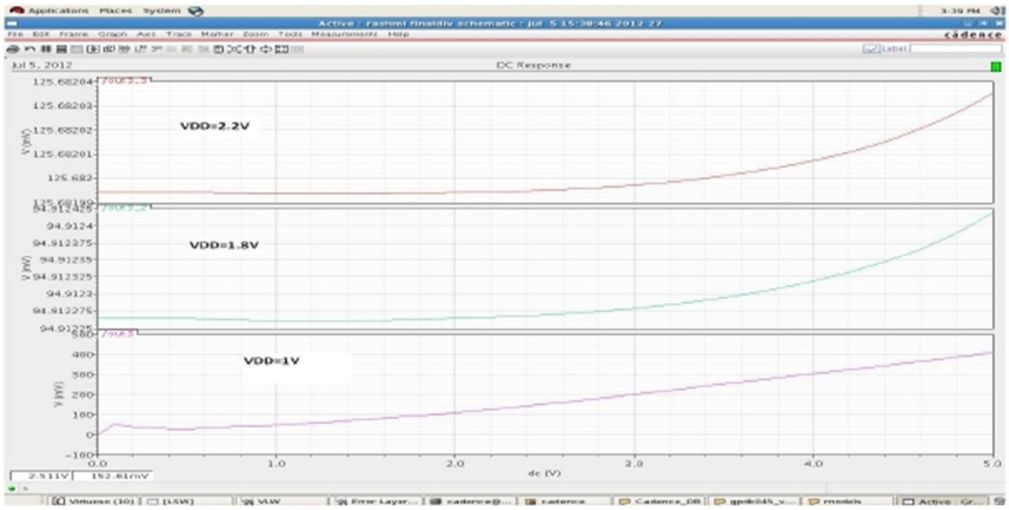

Figure 8 DC analysis of output voltage for different values of Vdd

TABLE I. POWER CONSUMPTION AND MAXIMUM OPERATING FREQUENCY FOR SEVERAL CMOS STATIC FREQUENCY DRIVERS

Ref	Vdd	Power(mW)	Max.Frequency	Technology
[7]	1.5	60.9	25	120nmCMOS
[8]	1.5	45	27	120nmCMOS
[9]	1.5	66	18.5	120nmCMOS
[10]	1.0	2.7	25	120nm SOI
Proposed	1.0	2.5	60	45nm CMOS

III. Conclusion

By optimizing transistor sizes in MSFF a power efficient 8:1 static divider in 45nm CMOS process is presented. The first 2:1 stage can work up to 60 GHz with only 2.5 mW power at 1.2-V supply.

References

[1] Krishnan, Z. Griffith, M. Urteaga, Y. Wei, D. Scot M. Dahlstrom, N. Parthasarathy, and M. Rodwell, "87 GHz static frequency divider in a InP-based mesa DHBT technology," in 24th Annu. GaAs IC Symp. Technical Dig., 2002, pp. 294–296

[2] H. Knapp, M. Wurzer, T. F. Meister, K. Aufinger, J. Bock, S. Boguth, and H. Schafer, "86 GHz static and 110 GHz dynamic frequency divider in SiGe bipolar technology," in IEEE MTT-S Dig., 2003, pp. 1067–1070

[3] H. Wu and A. Hajimiri, "A 19 Hz 0.5 mW 0.35 _m CMOS frequency divider with shunt-peaking locking-range enhancement," in ISSCC Tech. Dig., Feb. 2002, pp. 412–413.

[4] M.Wetzel et al., "A 26.5 GHz silicon MOSFET 2:1 dynamic frequency divider," IEEE Microw. Guided Wave Lett., vol. 10, no. 10, pp.221–223, Oct. 2000

[5] L. Lee and B. Razavi, "A 40-GHz frequency divider in 0.18-_mCMOS technology," IEEE J. Solid-State Circ., vol. 39, no. 4, pp. 594–601,Apr. 2004.

[6] B. A. Floyd and K. K. O, "SOI and bulk CMOS frequency divider Operating above 15 GHz," Electron. Lett., vol. 37, no. 10, pp. 617–618, May 2001

[7] H. Knapp, H.-D. Wohlmuth, M. Wurzer, and M. Rest, "25 GHz static frequency divider and 25 Gb/s multiplexer in 0.12 _mCMOS," in ISSCC Dig. Tech. Papers, Feb. 2002, pp. 302–303.

[8] H.-D.Wohlmuth and D. Kehrer, "A high sensitivity static 2:1 frequency divider up to 27 GHz in 120 nm CMOS," in Proc. Eur. Solid-State Circuit Conf. (ESSCIRC'02), 2002, pp. 823–826

[9] H.-D. Wohlmuth, D. Kehrer, and W. Simbourger, "A high sensitivity static 2:1 frequency divider up to 19 GHz in 120 nm CMOS," in Proc. IEEE RFIC, 2002, pp. 231–234

[10] J.-O. Plouchart, J. Kim, H. Recoulers, N. Zamdmer, Y. Tan, M. Sherony, A. Ray, and L. Wagner, "A power-efficient 33 GHz 2:1 static frequency divider in 0.12-_m SOI CMOS," in Proc. IEEE RFIC, 2003, pp. 329–332.